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(54) **Method for sustaining cells and pixels of plasma panels, electro-luminescent panels, LCD's or the like and a circuit for carrying out the method**

Verfahren und Schaltung zur Erhaltung von Zellen und Bildelementen von Plasma-Anzeigen, Elektrolumineszenz-Anzeigen, Flüssigkristall- oder ähnlichen Anzeigen

Méthode et circuit pour entretenir des cellules et des éléments d'image d'affichages à plasma, d'affichages à électro-luminescence, à cristaux liquides ou similaires

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(73) Proprietor: **The Board of Trustees of the University of Illinois**
Urbana Illinois 61801 (US)

(72) Inventors:
- **Weber, Larry F.**
  Champaign, IL 61820 (US)
- **Warren, Kevin W.**
  Champaign, IL 61820 (US)
- **Wood, Mark B.**
  500 South Woods Cross, Utah 84087 (US)

(74) Representative: **MEISSNER, BOLTE & PARTNER**
Patentanwälte
Postfach 86 06 24
81633 München (DE)

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- **HEWLETT-PACKARD JOURNAL vol. 36, no. 10, October 1985, PALO ALTO US pages 12 - 17, XP48118 M.L.HIGGINS 'High-Quality Electroluminescent Display for a Personal Workstation'**
- **1987 INTERNATIONAL SYMPOSIUM OF THE SOCIETY FOR INFORMATION DISPLAY, DIGEST OF TECHNICAL PAPERS vol. 18, 12 May 1987, NEW ORLEANS pages 92 - 95 L.F.WEBER ET AL. 'Energy Recovery Sustain Circuit for the AC Plasma Display'**

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Description

This invention relates to a method for sustaining cells and pixels of plasma panels, plasma display panels, electroluminescent panels, LCD's or the like and a circuit for carrying out the method.

BACKGROUND OF THE INVENTION

Plasma display panels, or gas discharge panels, are well known in the art and, in general, comprise a structure including a pair of substrates respectively supporting thereon column and row electrodes each coated with a dielectric layer such as a glass material and disposed in parallel spaced relation to define a gap therebetween in which an ionized gas is sealed. Moreover, the substrates are arranged such that the electrodes are disposed in orthogonal relation to one another thereby defining points of intersection which in turn define discharge cells at which selective discharges may be established to provide a desired storage or display function. It is also known to operate such panels with AC voltages and particularly to provide a write voltage which exceeds the firing voltage at a given discharge point, as defined by a selected column and row electrode, thereby to produce a discharge at a selected cell. The discharge at the selected cell can be continuously "sustained" by applying an alternating sustain voltage (which, by itself is insufficient to initiate a discharge). This technique relies upon the wall charges which are generated on the dielectric layers of the substrates which, in conjunction with the sustain voltage, operate to maintain discharges.

Details of the structure and operation of such gas discharge panels or plasma displays are set forth in US-A-3,559,190 issued January 26, 1971 to Donald L. Bitzer, et al.

In the past two decades, AC plasma displays have found widespread use due to their excellent optical qualities and flat panel characteristics. These qualities have made plasma displays a leader in the flat-panel display market. However, plasma panels have gained only a small portion of their potential market because of competition from lower costs CRT products.

The expense of the display electronics, not the display itself, is the most significant cost factor in plasma displays. Because of the matrix addressing schemes used, a separate voltage driver is required for each display electrode. Therefore, a typical 512X512 pixel display requires a total of 1024 electronic drivers and connections which add considerable bulk and cost to the final product.

In US-A-4 772 884 (U.S. Patent Application Serial Number 787,541 filed October 15, 1985), and assigned to the same assignee as herein, there is described an Independent Sustain and Address (ISA) plasma panel. Also, see the publication L.F. Weber and R.C. Younce, "Independent Sustain And Address Technique For The AC Plasma Display", 1986 Society For Information Display International Symposium Conference Record, pp. 220-223, San Diego, May, 1986. The ISA plasma panel technique includes the addition of an independent address electrode between the sustain electrodes. These address electrodes are then connected to the address drivers. The sustain electrodes can be bused together and connected directly to the sustainers.

The ISA plasma panel offers two significant advantages. First, since the address electrodes do not have to deliver the large sustain current to the discharging pixels, the address drivers have low current requirements. This allows lower cost drivers to be used. The second advantage is that only half the number of address drivers are needed since one address electrode can serve the sustain electrode on either side.

Despite the significant advantages afforded by the ISA panel, it is still desired to reduce as much as possible the manufacturing cost of such panels. However, while the ISA panel has enabled a reduction of the address drivers of a typical 512X512 pixel display from 1024 electronic address drivers to only 512 drivers, this is still a significant number of required electronic components. In fact, the plasma panel cost is dominated by the cost of the associated required electronic circuits such as the addressing driver circuits and sustain driver circuits. In addition, it is desired to reduce the amount of energy normally lost in charging and discharging the capacitance of the plasma panel.

It is therefore the object of the invention to provide a method and a circuit to reduce the cost and operational cost of plasma panels, plasma display panels, electroluminescent panels, LCD's or the like by reducing the cost/operational cost of the associated electronics.

SUMMARY OF THE INVENTION

The general concept of the present invention is based on the fact that plasma panels as described above comprise a panel capacitance which needs to be charged and decharged for sustaining stored information.

In accordance with the present invention, a sustaining method and a power efficient sustainer circuit have been developed for use with flat panels having substantial inherent panel capacitance due to the panel electrodes, such as plasma display panels, electroluminescent panels, liquid crystal displays, etc. The new sustain driver circuit uses inductors in charging and discharging the panel capacitance so as to recover 90% of the energy normally lost in driving the panel capacitance. Accordingly, a plasma panel incorporating a power efficient sustain driver circuit according to

the present invention can operate with only 10% of the energy normally required with prior art plasma panel sustaining circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a, 1b, 1c are schematic representations of switch devices useful in explaining an address circuit driver;

Figure 2 is a plan view of a plasma panel with open-drain address drivers and sustain drivers;

Figure 3 are waveform diagrams useful in understanding the operation of Figure 2;

Figure 4 are waveform diagrams showing an expanded view of the section of Figure 3 labeled 4-4;

Figure 5 is a schematic circuit diagram showing an ideal model of a new sustain driver according to the invention;

Figure 6 are waveform diagrams useful in understanding the operation of Figure 5;

Figure 7 is a schematic circuit diagram showing a practical circuit model of a new sustain driver according to the invention;

Figure 8 are waveform diagrams useful in understanding the operation of Figures 7 and 9;

Figure 9 and 9a are schematic circuit diagrams showing a constructed embodiment of a new sustain driver according to the invention;

Figure 10 is a schematic circuit diagram of a new sustain driver in an integrated circuit design;

Figure 11 is a schematic circuit diagram of an XAP address pulse driver incorporating energy recovery techniques according to the invention;

Figure 12 are waveform diagrams useful in understanding the operation of Figure 11;

Figure 13 is a schematic circuit diagram of YAP address pulse driver incorporating energy recovery techniques according to the invention; and

Figure 14 are waveform diagrams useful in understanding the operation of Figure 13.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention will be described in connection with an ISA plasma panel to which has been incorporated an address driver circuit and a new power efficient sustain driver circuit in accordance with the present invention. For convenience of description, an address driver circuit will be described briefly followed by the description of the power efficient sustain driver circuit of the present invention.

ISA Driver Circuits For Plasma Panels

Figure 1 shows the basic type of address circuit driver that can be used in plasma panel circuits. Figure 1a shows a simple switch in parallel with a diode. The switch is used to apply selective address pulses to the plasma panel depending on the state (open or closed) of the switch. With today's solid state switching technology, this switch usually takes two forms: the MOS Field Effect Transistor (MOSFET), shown in Figure 1b and the Bipolar transistor shown in Figure 1c.

Figure 2 shows a circuit diagram to drive the address electrodes in an ISA plasma panel i.e., a plasma display panel having independent sustain and address electrodes as previously. This example uses the N-channel MOSFET devices shown in Figure 1b, but of course other suitable switches could be used. The basic concept is to connect the drain electrode of each MOSFET to each address electrode of the ISA plasma panel and to then connect all of the sources of the MOSFETs on a given display axis to a common bus.

Figure 3 shows the waveforms used to drive the ISA panel. This shows a portion of the video scan of the panel for addressing the eight rows of pixels shown in Figure 2 in a top to bottom sequence. Other scanning techniques may

be used rather than the video scan example illustrated here. Each row of pixels requires two of the 20 microseconds addressing cycles. The top four waveforms show the signals applied by the four sustainers. The phasing of these waveforms selects which of the four pixels surrounding each address cell in Figure 2 can be addressed during a given addressing cycle. The fundamental periodicity of this phasing is every eight addressing cycles because of the sustain electrode connection technique used in Figure 2.

Below the sustain waveforms are the signals associated with the address electrodes. The waveforms labeled XAP and YAP are supplied from address pulse generators that are connected to the common bus of the address driver transistors as shown in Figure 2. These address pulsers generate the special waveforms needed for the address drivers to apply the proper signals to the address electrodes. The XA waveform shows the selective erase signals on the X address electrodes. A high XA level will erase a selected pixel and a low level leaves the pixel on. The YA waveforms for four adjacent Y address electrodes are shown at the bottom of Figure 3.

One concern is that when the column drivers are in a high impedance state, the pulses applied to a neighboring electrode in the low impedance state will capacitively couple to the high impedance electrode and cause it to receive the wrong voltage amplitude. This is not a significant problem for two reasons. First, note that in Figure 2, the address electrodes are shielded from each other by the sustain electrodes. This makes the variations in pulse amplitude, due to address line-to-line coupling, less than 10% of the address pulse amplitude as shown in Figure 4. The second point is that this 10% variation is not a significant problem because of the excellent address margins of the ISA design.

The energy recovery technique described hereinafter with respect to the power efficient sustain driver circuit can be used for the XAP and YAP address pulse generators to supply the waveforms of Figure 3.

Power Efficient Sustain Drive Circuit

The plasma panel requires a high voltage driver circuit called a sustainer, or sustain driver circuit, which drives all the pixels and dissipates considerable power. As an example, four sustainer drivers XSA, XSB, YSA, YSB are shown in Figure 2 with the ISA panel.

The following describes a new high efficiency sustainer that eliminates most of the power dissipation resulting from driving the plasma panel with a conventional sustainer. With this new sustainer, considerable savings can be realized in the overall cost of the plasma panel. The new sustainer can be applied to standard plasma panels, or the new ISA plasma panel, as well as to other types of display panels requiring a high voltage driver, such as electroluminescent or liquid crystal panels having inherent panel capacitance.

When the plasma panel is used as a display, frequent discharges are made to occur by alternatively charging each side of the panel to a critical voltage, which causes repeated gas discharges to occur. This alternating voltage is called the sustain voltage. If a pixel has been driven "ON" by an address driver, the sustainer will maintain the "ON" state of that pixel by repeatedly discharging that pixel cell. If a pixel has been driven "OFF" by an address driver, the voltage across the cell is never high enough to cause a discharge, and the cell remains "OFF".

The sustainer must drive all of the pixels at once; consequently, the capacitance as seen by the sustainer is typically very large. In a 512x512 panel, the total capacitance of all the pixel cells in the panel, Cp, could be as much as 5 nF.

Conventional sustainers drive the panel directly, and thus $1/2CpV_s^2$ is dissipated in the sustainer when the panel is subsequently discharged to ground. In a complete sustain cycle, each side of the panel is charged to Vs and subsequently discharged to ground. Therefore, a total of $2CpV_s^2$ is dissipated in a complete sustain cycle. The power dissipation in the sustainer is then $2CpV_s^2f$, where f is the sustain cycle frequency. For Cp = 5nF, Vs = 100 V, and f = 50 kHz, the power dissipation in the sustainer, resulting from driving the capacitance of the panel, is 5 W.

If an inductor is placed in series with the panel, then Cp can be charged and discharged through the inductor. Ideally, this would result in zero power dissipation since the inductor would store all of the energy otherwise lost in the output resistance of the sustainer and transfer it to or from Cp. However, switching devices are needed to control the flow of energy to and from the inductor, as Cp is charged and discharged. The "ON" resistance, output capacitance, and switching transition time are characteristics of the switching devices that can result in significant energy loss. The amount of energy that is actually lost due to these characteristics, and hence the efficiency, is determined largely by how well the circuit is designed to minimize these losses.

In addition to charging and discharging Cp, the sustainer must also supply the large gas discharge current for the plasma panel. This current, I, is proportional to the number of pixels that are "ON". The resulting instantaneous power dissipation is I^2R, where R is the output resistance of the sustainer. Thus, the power dissipation due to the discharge current is proportional to I^2, or the square of the number of pixels that are "ON".

There are two ways to minimize this dissipation. One is to minimize the output resistance of the sustainer by using very low resistance output drivers, and the other is to minimize the number of pixels that are "ON" at any time.

This invention provides a new sustainer circuit that will recover the energy otherwise lost in charging and discharging the panel capacitance, Cp. The efficiency with which the sustainer recovers this energy is here defined as the "recovery" efficiency. When Cp is charged to V_s and then discharged to zero, the energy that flows into and out of Cp

is $2CpV_s^2$; therefore, the recovery efficiency is defined by

$$Eff = 100x(2CpV_s^2-E_{lost})/2CpV_s^2$$

$$= 100x(1-(E_{lost}/2CpV_s^2)) \text{ percent}$$

where E_{lost} is the energy lost in charging and discharging Cp.

Notice that the recover efficiency is not the same as the conventional power efficiency, defined in terms of the power delivered to a load, since no power is delivered to the capacitor, Cp; it is simply charged and then discharged. The recovery efficiency is a measure of the energy loss in the sustainer.

A circuit proposed for driving electroluminescent (EL) panels, published in M.L. Higgins, "A Low-power Drive Scheme for AC TFEL Displays", SID International Symposium Digest of Technical Papers, Vol. 16, pp. 226-228, 1985, was tested in the laboratory, but was abandoned since it was not capable of better than 80% energy recovery, and it has undesirable design complexities. A new, very efficient sustain driver was then developed which eliminates the problems inherent in the prior proposed circuit.

First, a circuit model of the new sustain driver circuit will be analyzed to determine the expected recovery efficiency. The reasons why greater than 90% recover efficiency is possible with this new sustain driver will be explained, and several design guidelines will be given. Next, a constructed prototype of the new sustain driver will be discussed.

An ideal sustain driver circuit will be presented first to show the basic operation of the new sustain driver, given ideal components. As would be expected, given ideal components, this circuit has 100% recovery efficiency in charging and discharging a capacitative load. The schematic of the ideal sustain driver circuit is shown in Figure 5, and in Figure 6 are shown the output voltage and inductor current waveform expected for this circuit as the four switches are opened and closed through the four switching states. The operation during these four switching states is explained in detail below, where it is assumed that prior to State 1, Vss is at Vcc/2 (where Vcc is the sustain power supply voltage), Vp is at zero, S1 and S3 are open, and S2 and S4 are closed.

The reason that Vss is at Vcc/2 will be explained, below, after the switching operation is explained:

State 1. To start, S1 closes, S2 opens, and S4 opens. With S1 closed, L and Cp form a series resonant circuit, which has a forcing voltage of Vss = Vcc/2. Vp then rises to Vcc, at which point I_L is zero, and D1 becomes reverse biased. Alternatively, diode D1 could be eliminated and S1 opened when Vp rises to Vcc (at the point where I_L is zero).

State 2. S3 is closed to clamp Vp at Vcc and to provide a discharge current path for any "ON" pixels.

State 3. S2 closes, S1 opens, and S3 opens. With S2 closed, L and Cp again form a series resonant circuit, which has a forcing voltage of Vss = Vcc/2. Vp then falls to ground, at which point I_L is zero, and D2 becomes reverse biased. Alternatively, diode D2 could be eliminated and S2 opened when Vp falls to zero (at the point where I_L is zero).

State 4. S4 is closed to clamp Vp at ground while an identical driver on the opposite side of the panel drives the opposite side to Vcc and a discharge current then flows in S4 if any pixels are "ON".

It was assumed above that Vss remained stable at Vcc/2 during the above charging and discharging of Cp. The reasons for this can be seen as follows. If Vss were less than Vcc/2, then on the rise of Vp, when S1 is closed, the forcing voltage would be less than Vcc/2. Subsequently, on the fall of Vp, when S2 is closed, the forcing voltage would be greater than Vcc/2. Therefore, on average, current would flow into Css. Conversely, if Vss were greater than Vcc/2, then on average, current would flow out of Css. Thus, the stable voltage at which the net current into Css is zero is Vcc/2.

In fact, on power up, as Vcc rises, if the driver is continuously switched through the four states explained above, then Vss will rise with Vc at Vcc/2.

If this were not the case, a regulated power supply would be needed to supply the voltage Vss. This would increase the overall cost of the sustain circuitry and could make this design less desirable.

The energy losses due to the capacitances and resistances inherent in the real devices, i.e., the switching devices, the diodes, and the inductor, can be determined by analysis of a practical circuit model shown in Figure 7. The switching devices are modeled by an ideal switch, an output capacitor, and a series "ON" resistor. The diodes (except Dc1 and Dc2) are modeled by an ideal diode, a parallel capacitor, and a series resistor, and the inductor is modeled by an ideal inductor and a series resistor.

Dc1 and Dc2 are ideal diodes. They are included to prevent V1 from dropping below ground and V2 from rising above Vcc. As will be shown below, if Dc1 and Dc2 were not included, then the voltages across C1, Cd2, C2, and Cd2 would be higher than otherwise, which would lead to additional energy losses.

The switching sequence of this circuit is the same as that of the ideal model shown in Figure 5. Figure 8 shows the voltage levels for Vp, V1, V_L, and V2 and the current levels for I_L, I1, and I2 during the four switching states. Again, it is assumed that Vss is stable at Vcc/2.

The recovery efficiency in the practical circuit model of Figure 7 can be determined below with reference to Figure

8. For example, the energy losses due to the capacitance of the switching devices (C1 and C2) and the diodes (Cd1 and Cd2) can be determined; then, the energy losses due to the resistances of the switching devices (R1 and R2), the diodes (Rd1 and Rd2), and the inductor (R_L) can be determined; and finally, the energy loss due to the finite switching time of the switching devices can be determined. In each case, reference can be made to the four switching states, shown in Figure 8.

To find the power dissipation resulting from the capacitances of the switching devices and the diodes, an account is made of all the $1/2CV^2$ loss. It is assumed that, initially, S1 and S3 are open, S2 and S4 are closed, V_L is at ground, and Vss is at Vcc/2.

State 1. To start, S1 closes and S4 opens. V1 and V_L then rise to Vss, and the voltages across Cd2 ($V2-V_L$) and across C1 (Vss-V1) both fall from Vss to zero. Thus, $C1Vss^2/2$ is dissipated in R1 and $Cd2Vss^2/2$ is dissipated in R1, Rd1, and R2. S2 then opens. With S1 closed, the series combination of R1, Rd1, L, and Cp is a series RLC circuit with a forcing voltage of Vss=Vcc/2. The waveforms are shown in Figure 8. As I_L falls to and crosses zero, then D1 becomes cut off and V_L begins to rise.

State 2. S3 is closed to clamp Vp at Vcc. (Notice that before S3 closes, Vp has not completely risen to Vcc, due to the damping that was caused by R1, Rd1, and R_L. Thus, when S3 is closed, Vp is pulled up to Vcc through S3, and a small amount of overshoot could occur if there were stray inductances present in the real circuit. This overshoot is shown in the waveform for Vp in Figure 8). I_L then becomes negative as C2 and Cd1 (V_L-V1) both rise from zero to Vss, at which point Dc2 becomes forward biased and I2 begins to flow. The energy in the inductor, when I2 begins to flow, is then $1/2(C2+Cd1)Vss^2$. This energy is dissipated in R_L, Rd2, and R3 as I2 falls to zero.

State 3. After the discharge current for any "ON" pixel cells has been supplied, then S2 closes and S3 opens. V2 and V_L then fall to Vss, and the voltages across Cd1 (V_L-V1) and across C2 (V2-Vss) both fall from Vss to zero. Thus, $C2Vss^2/2$ is dissipated in R2 and $Cd1Vss^2/2$ is dissipated in R2, Rd2, and R1. S1 then opens. With S2 closed, the series combination of R2, Rd2, R_L, L, and Cp is a series RLC circuit with a forcing voltage of Vss = Vcc/2. The waveforms are shown in Figure 8. As I_L rises to and crosses zero, then D2 becomes cutoff and V_L begins to fall.

State 4. S4 is closed to clamp Vp at ground. (Notice that before S4 closes, Vp has not completely fallen to ground, due to the damping that was caused by R2, Rd2, and R_L. Thus, when S4 is closed, Vp is pulled down to ground through S4, and a small amount of undershoot could occur if there were stray inductances present in the real circuit. This undershoot is shown in the waveform for Vp in Figure 8.) I_L then becomes positive as CCl and Cd2 are charged from the inductor. The voltages across C1 (Vss-V1) and across Cd2 ($V2-V_L$) both rise from zero to Vss, at which point Dc1 becomes forward biased and I1 begins to flow. The energy in the inductor when I1 begins to flow is then $1/2(C1+Cd2)Vss^2$. This energy is dissipated in R_L, Rd1, and R4 as I1 falls to zero.

Thus, it can be determined that the practical circuit model of Figure 7 results in a power loss of $(f)E_{lost} = 0.17$ W, where the sustain frequency is equal to f = 50 kHz. By comparison, if there were no energy recovery, then the normal loss from charging and discharging Cp would be $(f)CpVcc^2 = 2.5$ W. The recovery efficiency (as previously defined) of the circuit of Figure 7 is

$$Eff = 100x(1-(E_{lost}/CpVcc^2)) = 93\%$$

where Cp = 5 nF and Vcc = 100 V.

In summary, the practical circuit model of Figure 7 predicts that the new sustain diver will be capable of 93% recovery, assuming that the Q of the inductor is at least 80 and that the optimum tradeoff between switch output capacitance and "ON" resistance is realized.

The schematic of a constructed prototype sustain driver circuit is shown in Figure 9, and a complete parts list is given in Table 1.

It was found that the waveforms of the constructed circuit of Figure 9 correspond almost exactly with the waveforms of Figure 8 predicted from the circuit model of Figure 7.

Switches S1, S2, S3, and S4 in Figure 7 were previously described as being switched at the appropriate times to control the flow of current to and from Cp. In the prototype circuit of Figure 9, the power MOSFETs (T1, T2, T3, T4) replace the ideal switches of Figure 7 and must be switched at the appropriate times by real drivers to control the flow of current to and from Cp. Switching T1 and T2 at the appropriate times requires only that they are switched on the transition of Vi. Thus, only a single driver (Driver 1) is required. Switching T3 and T4 presents a more difficult problem, however, since in addition to being switched on the transition of Vi, they must also be switched whenever the inductor current crosses zero. This could have required that T3 and T4 be controlled with additional inputs to the Figure 9 circuit if it were not the case that V1 and V2 make voltage transitions whenever Vi makes a transition and shortly after the inductor current crosses zero. Thus, the switching of T3 and T4 is accomplished by using the transitions of V1 and V2 to switch the Drivers (2 and 3) in Figure 9 at the appropriate times and no additional inputs are required.

Switching the MOSFETs can be seen with reference to Figure 9 and the following description. When Vi rises, the

output of Driver 1 is switched "LOW" and the gates of T1 and T2 are driven "LOW" through the coupling capacitors, C_{g1} and C_{g2}. Thus, T1 is switched "ON", T2 is switched "OFF", and current begins to flow in the inductor to charge Cp. Also, D3 becomes forward biased and D4 is reverse biased. This causes Driver 2 to quickly switch "LOW", thus driving T4 "OFF", while Driver 3 is delayed from switching "LOW" until after Vp has risen. (As will be explained later, R1 and R2 are needed only during initial startup when Vcc power is first applied and before Vss has risen high enough for Drivers 2 and 3 to be switched from the changes in voltage of V1 and V2.)

Referring back to the end of State 1 in Figure 8, it can be seen that V2, in Figure 9 will begin to rise from Vss to Vcc shortly after the inductor current into Cp has fallen to zero, at which time, T3 must be switched "ON" to clamp Vp at Vcc. In Figure 9, when V2 rises, then the input of Driver 3 also rises, due to the current through the coupling capacitor C4. The output of Driver 3 then switches "LOW", and the gate of T3 is driven "LOW" throughout the coupling capacitor, C_{g3}. Thus, T3 is switched "ON" and clamps Vp to Vcc.

Later, when Vi falls, the output of Driver 1 is switched "HIGH" and the gates of T1 and T2 are driven "HIGH" through the capacitors, C_{g1} and C_{g2}. Thus, T1 is switched "OFF", T2 is switched "ON", and current begins to flow in the inductor to discharge Cp. Also, D4 becomes forward biased and D3 becomes reverse biased. This causes Driver 3 to quickly switch "HIGH", thus driving T3 "OFF", while Driver 2 is delayed from switching "HIGH" until after Vp has fallen.

When V1 begins to fall from Vss to ground, shortly after the inductor current flowing out of Cp has fallen to Zero (as at the end of State 3 in Figure 8), then the input of Driver 2 falls because of the coupling capacitor C3. The output of Driver 2 then switches "HIGH", and the gate of T4 is driven "HIGH". Thus, T4 is switched "ON" and clamps Vp to ground.

Notice that an external timing circuit is not needed to determine when to switch T3 and T4 because the switching occurs shortly after the inductor current crosses zero, independent of the rise or fall time of Vp. This leads to simple circuitry that is independent of variations in the inductance (L) or the panel capacitance (Cp) and is a significant advantage over prior proposed sustain drivers. It also makes it possible to drive the circuit with only one input, so that if the input becomes stuck ("HIGH" or "LOW"), T3 and T4 cannot both be "ON" simultaneously, which would result in the destruction of one or both of the devices.

Another advantage that this circuit has over prior proposed circuits is that T1, D1, T2 and D2 need only be 1/2 Vcc rather than the full Vcc voltage of prior circuits. Lower voltage switching devices, requiring lower breakdown voltages, are typically less costly to fabricate. This results in a lower parts cost for a discrete sustainer and lower integration costs for an integrated sustainer.

The resistors, R1 and R2 are provided for the case in which Vss is at a very low voltage, such as during initial power up of Vcc. In this case, the voltages V1 and V2 do not change enough to cause the Drivers 2 and 3 to switch. The resistors will cause the Drivers 2 and 3 to switch, after a delay time, which is determined by the value of the resistors and the input capacitance of the Drivers.

The reason it is necessary to switch the Drivers 2 and 3 during initial power up when Vss is very low, is as follows. In order for Vss to rise, it is first necessary to T3 to switch "ON" and bring Vp up to Vcc. Then, when T2 turns "ON", a current will flow from Cp to Css. If T4 is later switched "ON", thus clamping Vp to ground, then when T1 turns "ON", the current that flows out of Css will prevent Vss from rising above Vcc/2, and Vss will begin to stabilize at Vcc/2 after several cycles of charging and discharging Cp. Thus, Vss will not achieve the proper voltage unless T3 and T4 are switched "ON" by the action of R1 and R2 during power up.

The resistor, R3, is provided to discharge the source to gate capacitance of T3 when the supply voltage, Vcc, suddenly rises during power up. Without R3, the source to gate voltage of T3 would rise above threshold, as Vcc rises, and remain there, with T3 "ON", after Vcc has risen. Then, if T4 were switched "ON", a substantial current would flow through T3 and T4 and possibly destroy one or both of the devices.

TABLE 1

Part Name	Number	Description	Manufacturer
T1	IRF9530	p-channel power MOSFET	Inter. React.
T2	IRF510	n-channel power MOSFET	Inter. React.
T3	IRF9530	p-channel power MOSFET	Inter. React.
T4	IRF510	n-channel power MOSFET	Inter. React.
D1	11DQ05	power schottky diode	Inter. React.
D2	11DQ05	power schottky diode	Inter. React.
D3	IN3070	high voltage diode	Texas Instru.
D4	IN3070	high voltage diode	Texas Instru.
Dc1	IN3070	high voltage diode	Texas Instru.
Dc2	IN3070	high voltage diode	Texas Instru.

TABLE 1 (continued)

Part Name	Number	Description	Manufacturer
INV	MM74CO4	CMOS inverter	Nat. Semicon.
Td1	MPS6531	NPN transistor	Motor. Semicon.
Td2	MPS6534	PNP transistor	Motor. Semicon.
L		2 µH air coil	J.W. Miller
Cp		5 nF silver mica cap	
Css		1 µF/ 50 volt cap	
C3		10 pF silver mica cap	
C4		10 pF silver mica cap	
Cg1		.01 µF/ 100 volt cap	
Cg2		.01 µF/ 100 volt cap	
Cg3		.01 µF/ 100 volt cap	
R1		100K ohm 1/4 watt	
R2		100K ohm 1/4 watt	
R3		33K ohm 1/4 watt	
(All zener diodes shown are 12 volt).			

In an experimental setup for measuring the efficiency of the prototype circuit in Figure 9, the supply voltage (Vcc) and the supply current were accurately measured while the circuit was driving a 5 nF capacitor load (Cp). The load was driven at a frequency of f = 5 kHz, with the supply voltage at 100 V. Thus, the normal power dissipation expected in this case was

$$P_{lost} = (\text{energy lost to charge Cp + energy lost to discharge Cp}) \text{ xf}$$

$$= (1/2CpVcc^2 + 1/2CpVcc^2) \text{ xf} = 2.5 \text{ W}$$

The measured supply current for the Figure 9 circuit was 2.0 mA, so the actual power drawn from the supply and dissipated in the driver was 0.2 W. Thus, this circuit recovered all but 0.2 W of the normally lost power. The previously defined recovery efficiency is therefore 92%.

By comparison, the recovery efficiency predicted by analysis of the circuit model of Figure 7 is 93%. This is an indication that the most significant sources of power loss in the real circuit of Figure 9 have been accurately accounted for in the model of Figure 7, and the model is a valid representation of the real circuit.

The sustain driver of Figure 9 can be used on each side of an ISA plasma panel. As an example, each of the sustain drivers XSA, XSB, YSA, YSB, in Figure 2 could be a sustain driver of Figure 9, and could be used with the open-drain address drivers previously described in connection with Figures 1-4.

After testing two sustain drivers (each as shown in Figure 9 with capacitor loads, one sustain driver was connected to each side of a 512x512 ac plasma display panel. It was found that these sustain drivers could drive the panel with 90% recovery efficiency when no pixels were "ON", and that with all of the pixels "ON", the dissipation was still low enough that heat sinks were not necessary. With all of the pixels "ON", the power dissipation in T1 and T2 did not change, but the power dissipation in T3 and T4 increased due to the I^2R losses resulting from the flow of discharge current. This power dissipation can be lowered by using lower "ON" resistance devices for T3 and T4.

In testing the prototype sustain driver circuit of Figure 9, it was found that this circuit continued to charge and discharge the panel at the sustain frequency with high recovery efficiency, regardless of large variations in the panel capacitance or in the inductance of the coil. This is a distinct advantage over prior proposed sustain driver circuits.

It may be possible to substitute bipolar power transistors for the power MOSFETs, T1 and T2 in Figure 9 in a suitably designed circuit. Also, since the power dissipation and, hence, the cooling requirements have been significantly reduced in the sustain driver circuit of Figure 9, if all of the sustainer electrodes can be economically integrated onto a single silicon chip, then the complete sustainer can be packaged into a single case with one heat sink.

With reference to Figure 10, there is illustrated an integrated, power efficient sustain driver circuit according to the invention that does not require resistors or capacitors. In the circuit of Figure 10, T1 and T2 are driven directly by the Level Shifter, T3 is driven directly from the CMOS Driver Dr1, and T4 is driven directly from the CMOS driver Dr2. If

Css1, Css2 and the inductor are excluded from integration, then the integrated circuit is made up entirely of active components. Thus, the silicon area required is minimized.

The operation of this circuit is basically the same as the circuit of Figure 9. As before, T1 and T2 charge and discharge Cp via L, and T3 and T4 clamp Vp at Vcc and ground, respectively. The difference is in the gate drive circuits Dr1, Dr2, and the Level Shifter, and in the addition of Css1.

Css1 and Css2 form a voltage divider where Css1 = Css2. Thus, at power up, when Vcc begins to rise, Vss will rise at Vcc/2. Later, when Vss has risen above the threshold level of the MOSFETs, then Vss will be held at Vcc/2.

The Level Shifter is a set-reset latch, with its output at either Vcc or ground. When Vi switches "HIGH", the output of the Level Shifter drops to ground and forces -Vss across the gate to source of both T1 and T2. This turns T1 "ON" and T2 "OFF". The input to Dr2 is then forced to Vss, the output of Dr2 drops to ground, and T4 is turned "OFF". Later, when I_L falls to zero and then reverses, the input to Dr1 rises from Vss to Vcc, the gate of T3 is then pulled down by Dr1 to Vss, and T3 turns "ON". Thus, Vp is driven to Vcc when Vi switches "HIGH".

When Vi switches "LOW", the output of the Level Shifter rises to Vcc and forces Vss across the gate to source of both T1 and T2. This turns T1 "OFF" and T2 "ON". The input to Dr1 is then forced to Vss, the output of Dr1 rises to Vcc and T3 is turned "OFF". Later when I_L falls to zero and then reverses, the input to Dr2 falls from Vss to ground. The gate of T4 is then driven up by Dr2 to Vss, and T4 turns "ON".

The XAP and YAP address pulse generators may also be designed with the energy recovery technique previously described in connection with the sustain driver circuit. As an example, reference may be made to Figures 11-14. Figure 11 illustrates an XAP address pulse generator connected to the panel electrodes at the output terminal. Figure 12 illustrates the output voltage and inductor current waveforms (similar to Figures 5 and 6 with respect to the sustain driver) as switches S1 and S4 are opened and closed through the switching states. The output voltage waveform in Figure 12 is a positive double pulse conforming to the desired XAP waveforms of Figures 3 and 4. Notice that switch S2 of Figure 5 has been eliminated in the XAP generator of Figure 11 since diode D3, diode D2 and S2 in Figures 5 and 6.

Figure 13 illustrates YAP generator and Figure 14 illustrates the corresponding waveforms in the switching states. Capacitor C_D and the output capacitance connected to the output terminal function as a voltage divider of voltage Vcc supplied to the circuit. When a Write Pulse is required (See Figure 14), switch S5 is closed to short capacitor C_D to provide the full amplitude Write Pulse to the panel. If an Erase Pulse is required, switch S5 is opened to provide the reduced amplitude Erase Pulse to the panel.

If desired, an ISA panel can be provided with N-channel MOSFET address drivers on one axis and P-channel MOSFET address drivers on the other axis, using techniques similar to the YAP and XAP address driver circuit techniques previously described. For example, a YAP address pulse generator with an N-channel MOSFET driver could be used with negative pulse similar to the negative pulses of the YAP pulses in Figure 3. For the XAP address pulse generator a P-channel MOSFET driver could be used with a positive going single pulse having a pulse width equal to the width between the two double XAP pulses shown in the expanded view of Figure 4.

Claims

1. A method for sustaining cells and pixels of plasma panels, plasma display panels, electroluminescent panels, or LCDs having panel electrodes and corresponding panel capacitance in which the address cells and/or pixels are defined by the intersection of respective address electrodes in respective arrays of (X and Y dimension) address electrodes, said method employing an inductor (L) and
characterized by the steps of:

   charging the panel capacitance (Cp) through said inductor (L), initially while storing energy in said inductor (L) until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero;

   discharging the panel capacitance (Cp) through said inductor (L), initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero,

   wherein said charging and/or discharging of the panel capacitance includes applying a forcing voltage (Vss) which is about one-half the magnitude of the voltage level (Vcc) the panel capacitance reaches after charging.

2. Method according to Claim 1, further including the steps of after charging/discharging the panel capacitance, maintaining the panel capacitance in a charged/ discharged state prior to again discharging/charging the panel capacitance (Cp).

3. Method according to Claim 2, wherein the step of maintaining the panel capacitance in a charged state includes clamping the voltage level (Vcc) of the panel capacitance (Cp) upon the inductor current reaching zero, and wherein the step of maintaining the panel capacitance (Cp)in a discharged state prior to again charging includes clamping the voltage level (Vcc) of the panel capacitance upon the inductor current reaching zero.

4. Circuit for sustaining cells and pixels of plasma panels, plasma display panels, electroluminescent panels, or LCDs having panel electrodes and corresponding panel capacitance in which the address cells and/or pixels are defined by the intersection of respective address electrodes in respective arrays of (X and Y dimension) address, comprising an inductor (L) coupled to the panel electrodes, and a driver circuit coupled to the inductor (L) for operating the display panel through the inductor (L),
characterized in that

the driver circuit includes means (Vss, S1 - S4) adapted to charge the panel capacitance through said inductor (L), initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero;

means (Vss, S1 - S4) adapted to discharge the panel capacitance through said inductor (L), initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum, and secondly while removing the stored energy from said inductor until the inductor current reaches zero; and

means for applying a forcing voltage (Vss) which is about one-half the magnitude of the voltage level (Vcc) the panel capacitance reaches after charging.

5. Circuit according to Claim 4, further comprising means (S1, S3) for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during charging of the panel capacitance;
second means (S2, S4) for clamping the voltage level to the panel capacitance upon the inductor current reaching zero during discharge of the panel capacitance.

6. Circuit according to Claim 5, wherein said first and second means for clamping includes means (Cd1, Cd2) responsive to the inductor current reaching zero to provide said clamping independent of variations in the values of said inductor or said panel capacitance.

7. Circuit according to Claim 4, 5 or 6, wherein said charging means include first switch means (S1) coupled to said inductor (L) to enable said panel capacitance (Cp) to charge through said inductor from a first voltage level (a) initially to an intermediate voltage level magnitude which is about one-half the desired voltage level magnitude, while storing energy in said inductor, and (b) then to said desired voltage level magnitude, while removing said stored energy from said inductor; and said discharging means includes second switch means (S2) coupled to said inductor (L) to enable said panel capacitance to discharge through said inductor from said desired voltage level magnitude (a) initially to an intermediate voltage level magnitude which is about one-half the desired voltage level magnitude, while storing energy in said inductor, and (b) then to said first voltage level magnitude, while removing said stored energy from said inductor.

8. Circuit according to one of Claims 4 to 7, further including switch means (S1 - S4) for maintaining the panel capacitance in a charged state after charging the panel capacitance prior to discharge and/or switch means (S1 - S4) for maintaining the panel capacitance in a discharged state after discharge or upon the inductor current reaching zero and prior to again charging the panel capacitance.

9. Circuit according to Claim 8, wherein said means for maintaining the panel capacitance in a charged state includes means for charging the voltage level (Vp) of the panel capacitance upon the inductor current reaching zero during charging of the panel capacitance, and wherein said means for maintaining the panel capacitance in a discharged state includes means (S2, S4) for clamping the voltage level of the panel capacitance upon the inductor current reaching zero during discharging of the panel capacitance (Cp).

Patentansprüche

1. Verfahren zur Erhaltung von Zellen und Bildelementen von Plasmaanzeigen, Plasma-Bildschirmen, Elektrolumineszenzanzeigen oder Flüssigkristallanzeigen, die Anzeigeelektroden und eine entsprechende Anzeigekapazität

haben, wobei die Adreßzellen und/oder -bildelemente durch den Schnittpunkt von jeweiligen Adreßelektroden in entsprechenden Arrays von Adreßelektroden (der X- und Y-Dimension) definiert sind und wobei das Verfahren einen Induktor (L) verwendet und
gekennzeichnet ist durch die folgenden Schritte:

Laden der Anzeigekapazität (Cp) durch den Induktor (L), und zwar anfänglich, während gleichzeitig Energie in dem Induktor (L) gespeichert wird, bis der Wert des Induktorstroms ein Maximum erreicht, und zweitens, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird, bis der Induktorstrom Null erreicht;

Entladen der Anzeigekapazität (Cp) durch den Induktor (L), und zwar anfänglich, während gleichzeitig Energie in dem Induktor gespeichert wird, bis der Wert des Induktorstroms ein Maximum erreicht, und zweitens, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird, bis der Induktorstrom Null erreicht,

wobei das Laden und/oder Entladen der Anzeigekapazität das Anlegen einer Stützspannung (Vss) aufweist, die ungefähr den halben Wert des Spannungspegels (Vcc) hat, den die Anzeigekapazität nach dem Laden erreicht.

2. Verfahren nach Anspruch 1, das ferner die folgenden Schritte aufweist: nach dem Laden/Entladen der Anzeigekapazität Halten der Anzeigekapazität in einem geladenen/entladenen Zustand, bevor die Anzeigekapazität (Cp) erneut entladen/geladen wird.

3. Verfahren nach Anspruch 2, wobei der Schritt des Haltens der Anzeigekapazität in einem geladenen Zustand das Begrenzen des Spannungspegels (Vcc) der Anzeigekapazität (Cp) aufweist, wenn der Induktorstrom Null erreicht, und wobei der Schritt des Haltens der Anzeigekapazität (Cp) in einem entladenen Zustand vor dem erneuten Laden das Begrenzen des Spannungspegels (Vcc) der Anzeigekapazität aufweist, wenn der Induktorstrom Null erreicht.

4. Schaltung zur Erhaltung von Zellen und Bildelementen von Plasmaanzeigen, Plasma-Bildschirmen, Elektrolumineszenzanzeigen oder Flüssigkristallanzeigen, die Anzeigeelektroden und eine entsprechende Anzeigekapazität haben, wobei die Adreßzellen und/oder bildelemente durch den Schnittpunkt von jeweiligen Adreßelektroden in entsprechenden Arrays von Adreßelektroden (der X- und Y-Dimension) definiert sind, wobei die Schaltung einen mit den Anzeigeelektroden gekoppelten Induktor (L) und eine Treiberschaltung aufweist, die mit dem Induktor (L) gekoppelt ist, um die Anzeige durch den Induktor (L) zu betreiben,
dadurch gekennzeichnet, daß

die Treiberschaltung folgendes aufweist: Einrichtungen (Vss, S1-S4), die ausgebildet sind, um die Anzeigekapazität durch den Induktor (L) zu laden, und zwar anfänglich, während gleichzeitig Energie in dem Induktor gespeichert wird, bis der Wert des Induktorstroms ein Maximum erreicht, und zweitens, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird, bis der Induktorstrom Null erreicht;

Einrichtungen (Vss, S1-S4), die ausgebildet sind, um die Anzeigekapazität durch den Induktor (L) zu entladen, und zwar anfänglich, während gleichzeitig Energie in dem Induktor gespeichert wird, bis der Wert des Induktorstroms ein Maximum erreicht, und zweitens, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird, bis der Induktorstrom Null erreicht; und

eine Einrichtung zum Anlegen einer Stützspannung (Vss), die ungefähr den halben Wert des Spannungspegels (Vcc) hat, den die Anzeigekapazität nach dem Laden erreicht.

5. Schaltung nach Anspruch 4, die ferner folgendes aufweist: eine Einrichtung (S1, S3) zum Begrenzen des Spannungspegels der Anzeigekapazität, wenn der Induktorstrom während des Ladens der Anzeigekapazität Null erreicht;
eine zweite Einrichtung (S2, S4) zum Begrenzen des Spannungspegels der Anzeigekapazität, wenn der Induktorstrom während des Entladens der Anzeigekapazität Null erreicht.

6. Schaltung nach Anspruch 5, wobei die erste und die zweite Einrichtung zum Begrenzen Elemente (Cd1, Cd2) aufweisen, die in Abhängigkeit davon, daß der Induktorstrom Null erreicht, die Begrenzung unabhängig von Änderungen der Werte des Induktors oder der Anzeigekapazität bewirken.

7. Schaltung nach Anspruch 4, 5 oder 6, wobei die Ladeeinrichtung eine erste Schalteinrichtung (S1) aufweist, die mit dem Induktor (L) gekoppelt ist, um der Anzeigekapazität (Cp) zu ermöglichen, sich durch den Induktor von einem ersten Spannungspegel aufzuladen, und zwar (a) anfänglich auf einen Zwischen-Spannungspegelwert, der ungefähr der halbe gewünschte Spannungspegelwert ist, während gleichzeitig Energie in dem Induktor gespeichert wird, und (b) dann auf den gewünschten Spannungspegelwert, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird; und die Entladeeinrichtung eine zweite Schalteinrichtung (S2) aufweist, die mit dem Induktor (L) gekoppelt ist, um der Anzeigekapazität zu ermöglichen, sich durch den Induktor von dem gewünschten Spannungspegelwert zu entladen, und zwar (a) anfänglich auf einen Zwischen-Spannungspegelwert, der ungefähr der halbe gewünschte Spannungspegelwert ist, während gleichzeitig Energie in dem Induktor gespeichert wird, und (b) dann auf den ersten Spannungspegelwert, während gleichzeitig die gespeicherte Energie von dem Induktor abgeleitet wird.

8. Schaltung nach einem der Ansprüche 4 bis 7, die ferner folgendes aufweist: Schalteinrichtungen (S1-S4), um die Anzeigekapazität in einem geladenen Zustand zu halten, nachdem die Anzeigekapazität vor dem Entladen geladen wurde, und/oder Schalteinrichtungen (S1-S4), um die Anzeigekapazität nach dem Entladen oder dann, wenn der Induktorstrom Null erreicht, und vor dem erneuten Laden der Anzeigekapazität diese in einem entladenen Zustand zu halten.

9. Schaltung nach Anspruch 8, wobei die Einrichtung zum Halten der Anzeigekapazität in einem geladenen Zustand Mittel aufweist, um den Spannungspegel (Vp) der Anzeigekapazität zu laden, wenn der Induktorstrom während des Ladens der Anzeigekapazität Null erreicht, und wobei die Einrichtung zum Halten der Anzeigekapazität in einem entladenen Zustand Mittel (S2, S4) aufweist, um den Spannungspegel der Anzeigekapazität zu begrenzen, wenn der Induktorstrom während des Entladens der Anzeigekapazität (Cp) Null erreicht.

Revendications

1. Procédé permettant d'entretenir des cellules et des éléments d'image de panneaux à plasma, panneaux afficheurs à plasma, panneaux électroluminescents ou panneaux à cristaux liquides ayant des électrodes de panneau et une capacité de panneau correspondante dans lesquels l'adresse des cellules et/ou éléments d'image est définie par l'intersection d'électrodes d'adressage respectives dans des matrices respectives d'électrodes d'adressage (de dimensions X et Y), ledit procédé employant une inductance (L) et étant caractérisé par les étapes consistant à :

   charger la capacité du panneau (Cp) par l'intermédiaire de ladite inductance (L), initialement en stockant de l'énergie dans ladite inductance (L) jusqu'à ce que la grandeur du courant dans l'inductance atteigne un maximum, et deuxièmement en retirant de l'énergie de ladite inductance jusqu'à ce que le courant dans l'inductance devienne nul ;
   décharger la capacité du panneau (Cp) par l'intermédiaire de ladite inductance (L), initialement en stockant de l'énergie dans ladite inductance jusqu'à ce que la grandeur du courant dans l'inductance atteigne un maximum, et deuxièmement en retirant de l'énergie de ladite inductance jusqu'à ce que le courant dans l'inductance devienne nul ;
   ladite charge et/ou décharge de la capacité du panneau comprenant l'application d'une tension de forçage (Vss) qui est égale à environ la moitié de la grandeur du niveau de tension (Vcc) atteint par la capacité du panneau après la charge.

2. Procédé selon la revendication 1, comprenant en outre les étapes consistant, après avoir chargé/déchargé la capacité du panneau, à maintenir la capacité du panneau dans un état chargé/déchargé avant de charger/décharger à nouveau la capacité du panneau (Cp).

3. Procédé selon la revendication 2, dans lequel l'étape consistant à maintenir la capacité du panneau à l'état chargé comprend la fixation du niveau de tension (Vcc) de la capacité du panneau (Cp) lorsque le courant dans l'inductance atteint zéro, et dans lequel l'étape consistant à maintenir la capacité du panneau (Cp) à l'état déchargé avant de la charger à nouveau comprend la fixation du niveau de tension (Vcc) de la capacité du panneau lorsque le courant dans l'inductance devient nul.

4. Circuit pour entretenir des cellules et des éléments d'image de panneaux à plasma, panneaux afficheurs à plasma, panneaux électroluminescents ou panneaux à cristaux liquides ayant des électrodes de panneau et une capacité de panneau correspondante dans lesquels l'adresse des cellules et/ou éléments d'image est définie par l'inter-

section d'électrodes d'adressage respectives dans des matrices respectives d'électrodes d'adressage (de dimensions X et Y), comprenant une inductance (L) couplée aux électrodes du panneau et un circuit de commande couplé à l'inductance (L) afin de faire fonctionner le panneau afficheur par l'intermédiaire de l'inductance (L),

caractérisé en ce que

le circuit de commande comprend des moyens (Vss, S1 à S4) adaptés pour charger la capacité du panneau par l'intermédiaire de ladite inductance (L), initialement en stockant de l'énergie dans ladite inductance jusqu'à ce que la grandeur du courant dans l'inductance atteigne un maximum, et deuxièmement en retirant de l'énergie de ladite inductance jusqu'à ce que le courant dans l'inductance devienne nul ;

des moyens (Vss, S1 à S4) adaptés pour décharger la capacité du panneau par l'intermédiaire de ladite inductance (L), initialement en stockant de l'énergie dans ladite inductance jusqu'à ce que la grandeur du courant dans l'inductance atteigne un maximum, et deuxièmement en retirant de l'énergie de ladite inductance jusqu'à ce que le courant dans l'inductance devienne nul ; et

des moyens pour appliquer une tension de forçage (Vss) qui est égale à environ la moitié de la grandeur du niveau de tension (Vcc) atteint par la capacité du panneau après la charge.

5. Circuit selon la revendication 4, comprenant en plus des moyens (S1, S3) pour fixer le niveau de tension de la capacité du panneau lorsque le courant dans l'inductance devient nul lors de la charge de la capacité du panneau ;

des seconds moyens (S2, S4) pour fixer le niveau de tension de la capacité du panneau lorsque le courant dans l'inductance devient nul lors de la décharge de la capacité du panneau ;

6. Circuit selon la revendication 5, dans lequel lesdits premiers et seconds moyens de fixation du niveau de tension comprennent des moyens (Cd1, Cd2) répondant au courant dans l'inductance devenant nul afin de fournir ladite fixation du niveau de tension indépendamment des variations des valeurs de ladite inductance ou de ladite capacité du panneau.

7. Circuit selon les revendications 4, 5 ou 6, dans lequel lesdits moyens de charge comprennent des premiers moyens de commutation (S1) couplés à ladite inductance (L) afin de permettre à ladite capacité du panneau (Cp) de se charger par l'intermédiaire de ladite inductance à partir d'un premier niveau de tension (a) initialement à une valeur de niveau de tension intermédiaire qui est égale à environ la moitié de la valeur de niveau de tension souhaitée, tout en stockant de l'énergie dans ladite inductance, et (b) ensuite à ladite valeur de niveau de tension souhaitée, tout en retirant ladite énergie stockée de ladite inductance ; et lesdits moyens de décharge comprennent des seconds moyens de commutation (S2) couplés à ladite inductance (L) afin de permettre à ladite capacité du panneau de se décharger à partir de ladite valeur de niveau de tension souhaitée (a) initialement à une valeur de niveau de tension intermédiaire qui est égale à environ la moitié de la valeur de niveau de tension souhaitée, tout en stockant de l'énergie dans ladite inductance, et (b) ensuite à ladite première valeur de niveau de tension, tout en retirant ladite énergie stockée de ladite inductance.

8. Circuit selon l'une quelconque des revendications 4 à 7, comprenant en outre des moyens de commutation (S1 - S4) pour maintenir la capacité du panneau à l'état chargé après avoir chargé la capacité du panneau avant la décharge et/ou des moyens de commutation (S1 - S4) pour maintenir la capacité du panneau à l'état déchargé après la décharge ou lorsque le courant dans l'inducteur devient nul et avant de charger à nouveau la capacité du panneau.

9. Circuit selon la revendication 8, dans lequel lesdits moyens de maintien de la capacité du panneau à l'état chargé comprennent des moyens pour fixer le niveau de tension (Vp) de la capacité du panneau lorsque le courant dans l'inductance devient nul pendant la charge de la capacité du panneau, et dans lequel lesdits moyens de maintien de la capacité du panneau à l'état déchargé comprennent des moyens (S2, S4) pour fixer le niveau de tension (Vp) de la capacité du panneau lorsque le courant dans l'inductance devient nul pendant la décharge de la capacité du panneau

FIG. 1

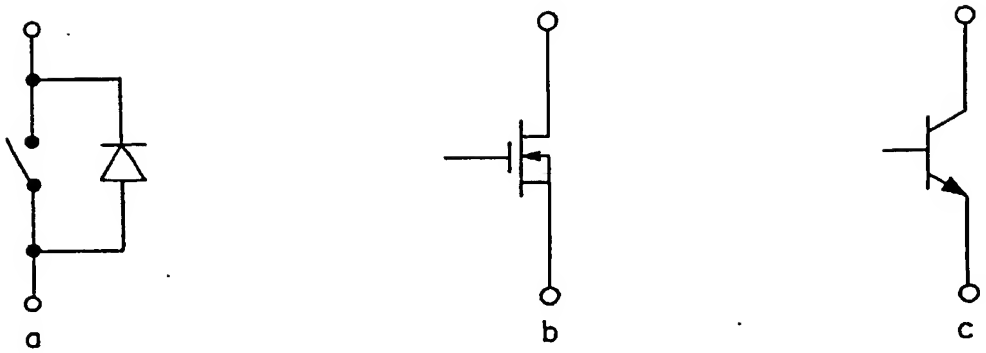

a
b
c

FIG. 2

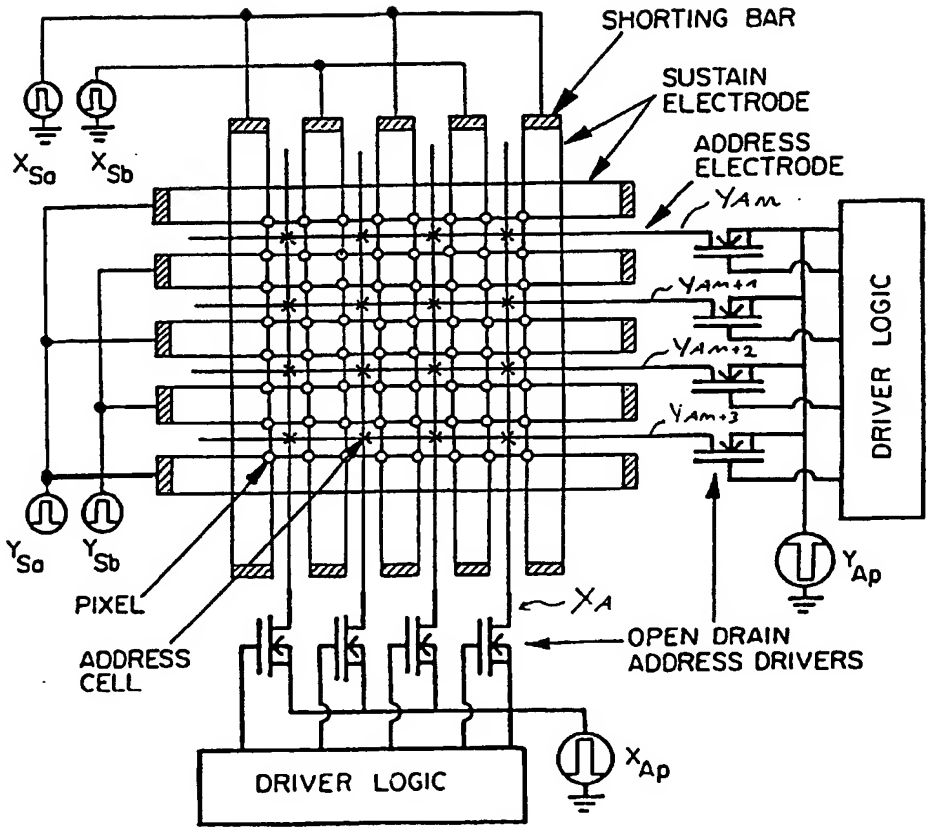

SHORTING BAR
SUSTAIN ELECTRODE
ADDRESS ELECTRODE
X_{Sa}
X_{Sb}
Y_{Am}
Y_{Am+1}
Y_{Am+2}
Y_{Am+3}
DRIVER LOGIC
Y_{Sa}
Y_{Sb}
Y_{Ap}
PIXEL
X_A
ADDRESS CELL
OPEN DRAIN ADDRESS DRIVERS
DRIVER LOGIC
X_{Ap}

FIG.3

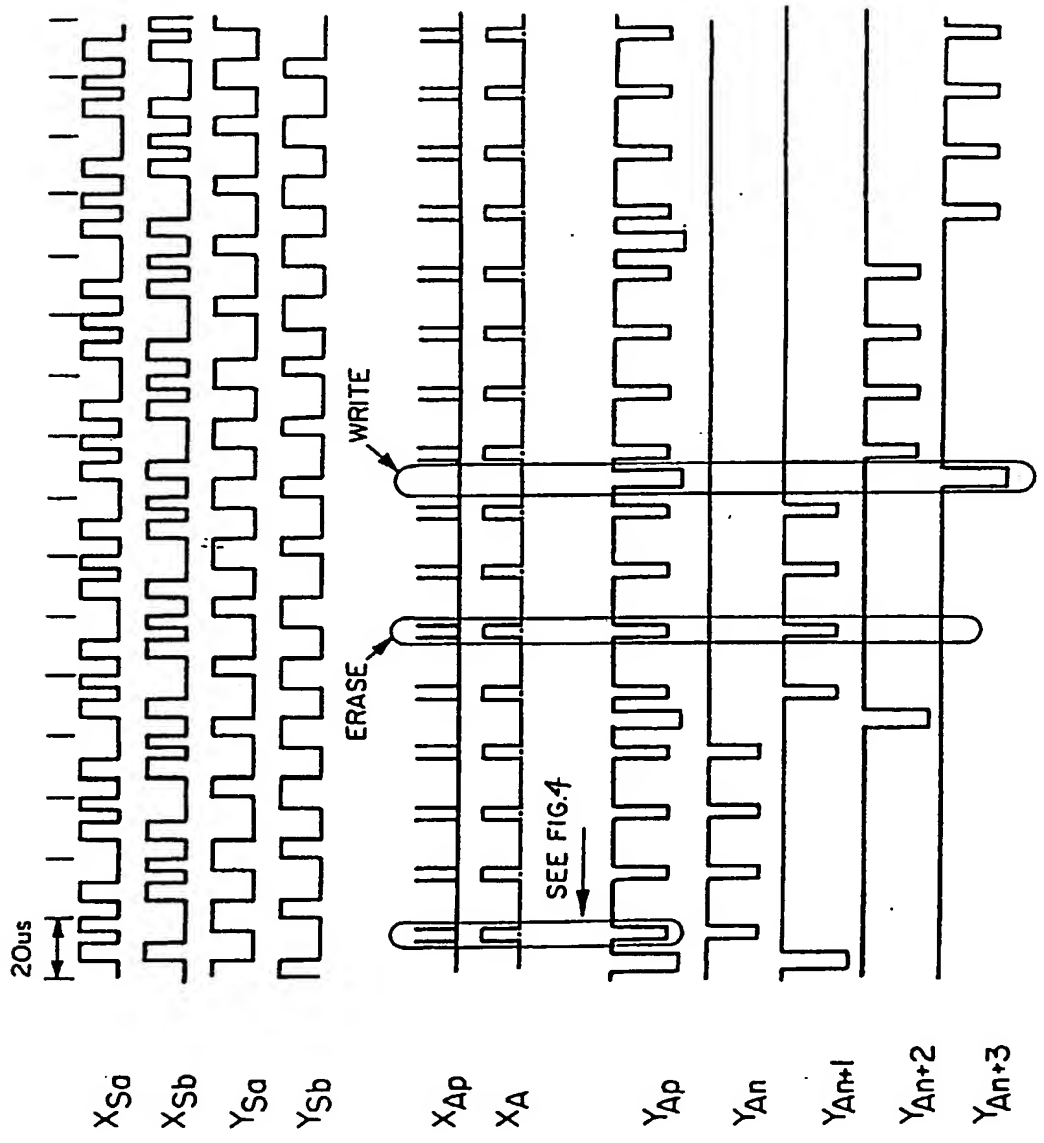

20us
WRITE
ERASE
SEE FIG.4
XSa
XSb
YSa
YSb
XAp
XA
YAp
YAn
YAn+1
YAn+2
YAn+3

FIG.4

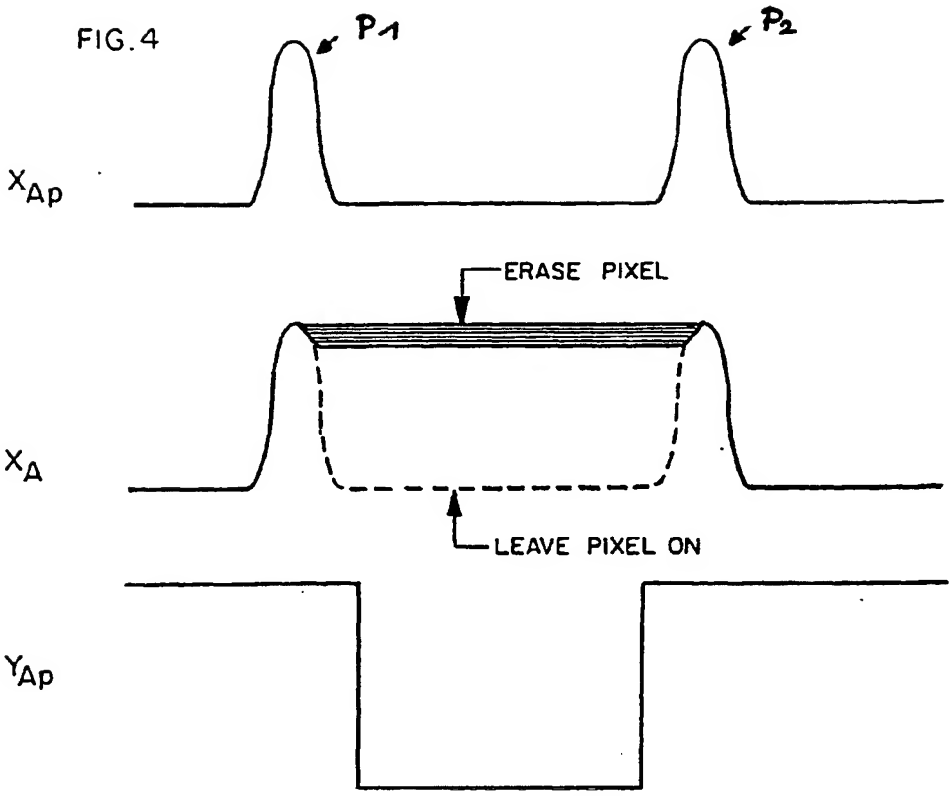

P1
P2
XAp
ERASE PIXEL
XA
LEAVE PIXEL ON
YAp

FIG.5

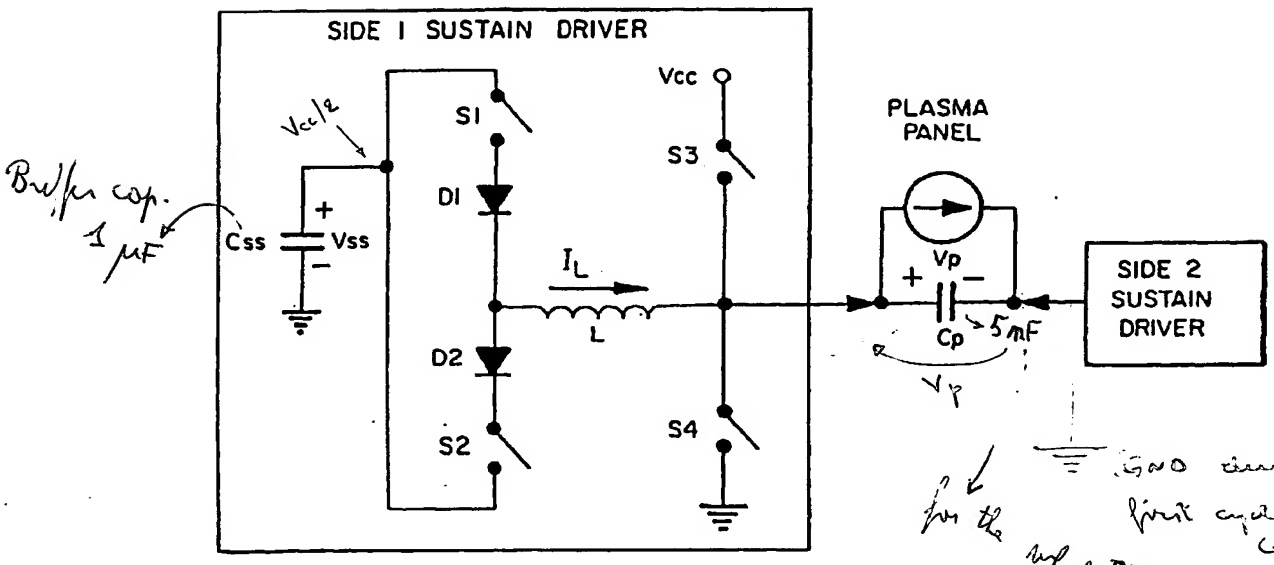

SIDE 1 SUSTAIN DRIVER
Vcc
S1
S3
Vcc/2
D1
Buffer cap.
1 μF
Css
Vss
IL
L
D2
S2
S4
PLASMA PANEL
Vp
Cp
5 nF
SIDE 2 SUSTAIN DRIVER
GND common
for the whole PDP panel!

FIG. 6

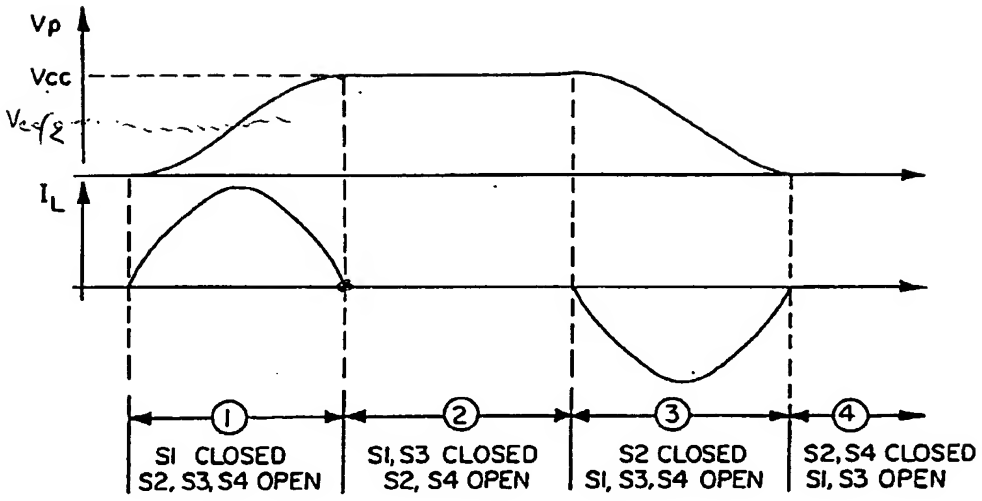

Vp
Vcc
Vref2
IL
1
2
3
4
S1 CLOSED
S2, S3, S4 OPEN
S1, S3 CLOSED
S2, S4 OPEN
S2 CLOSED
S1, S3, S4 OPEN
S2, S4 CLOSED
S1, S3 OPEN

FIG. 7

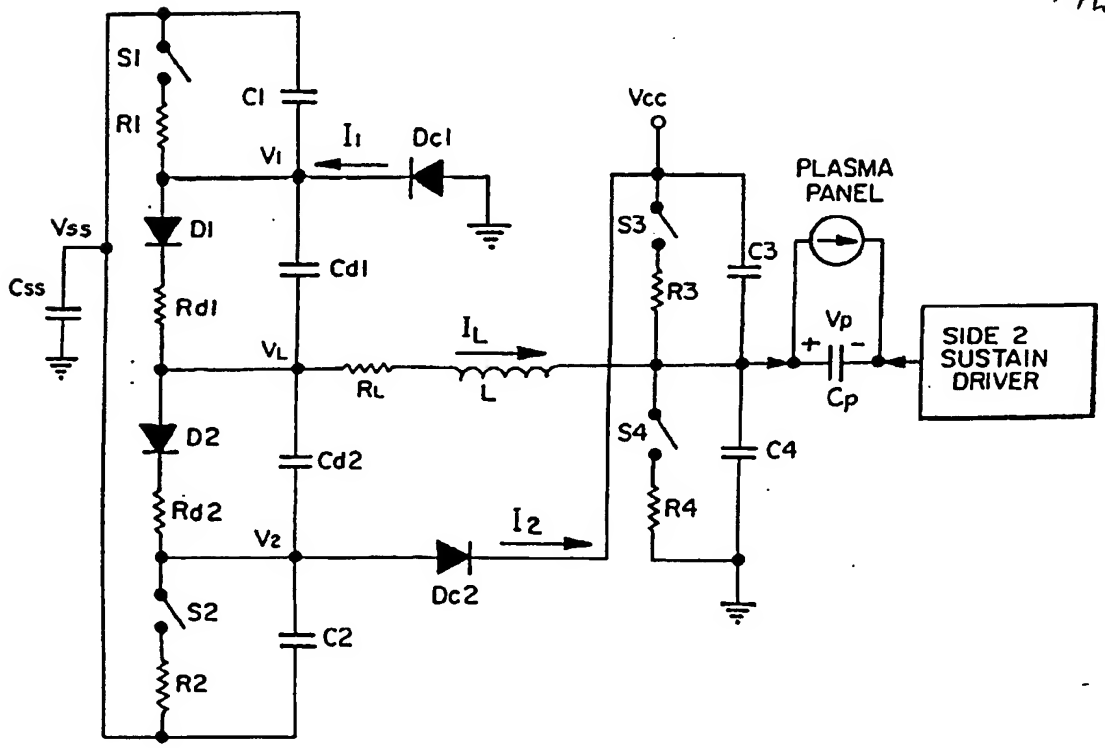

S1
R1
C1
V1
I1
Dc1
Vss
D1
Cd1
Css
Rd1
VL
IL
RL
L
D2
Cd2
Rd2
V2
I2
Dc2
S2
C2
R2
Vcc
S3
R3
C3
S4
R4
C4
PLASMA PANEL
Vp
Cp
SIDE 2 SUSTAIN DRIVER

FIG.8

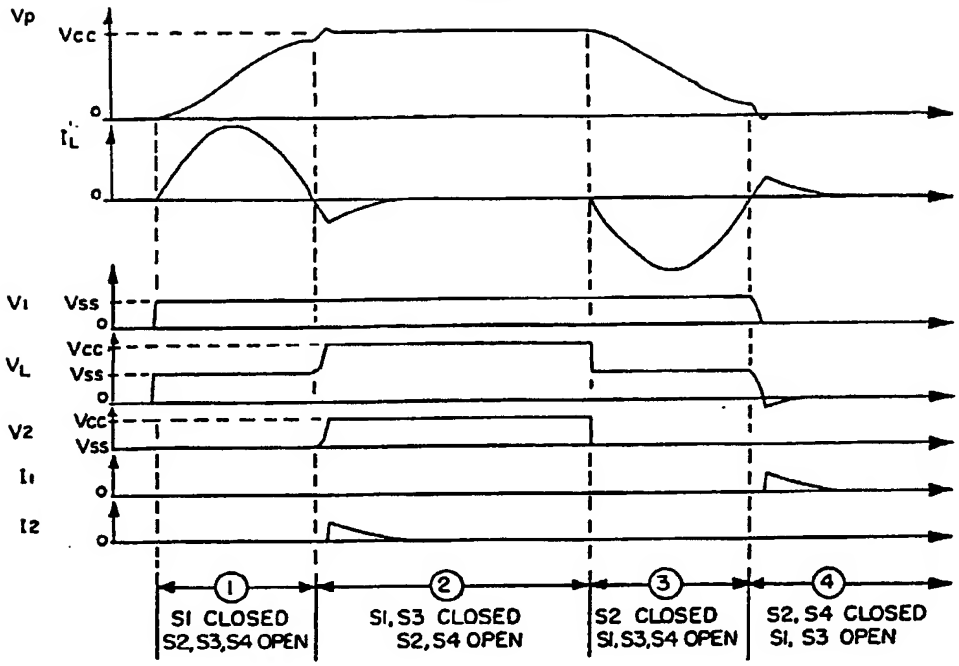
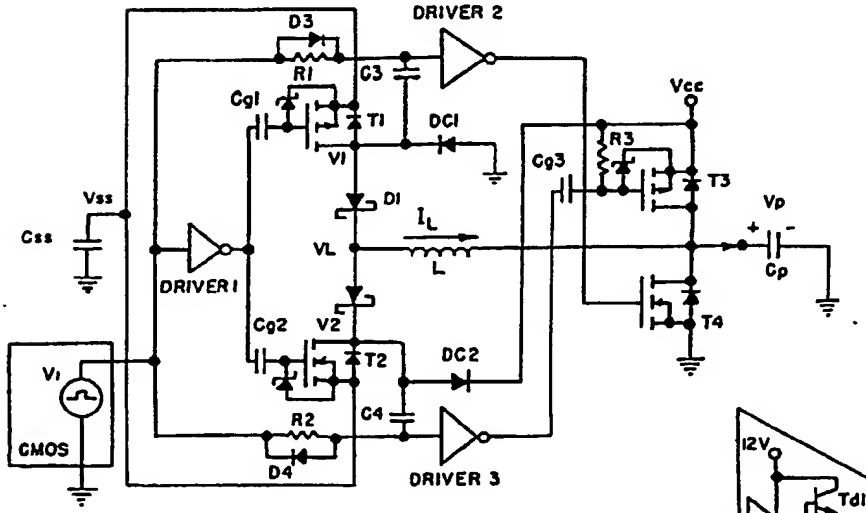


FIG.9



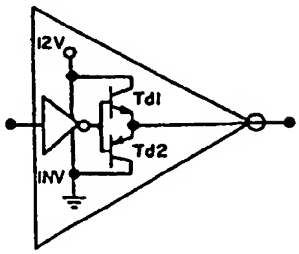


FIG. 9a

FIG. 10

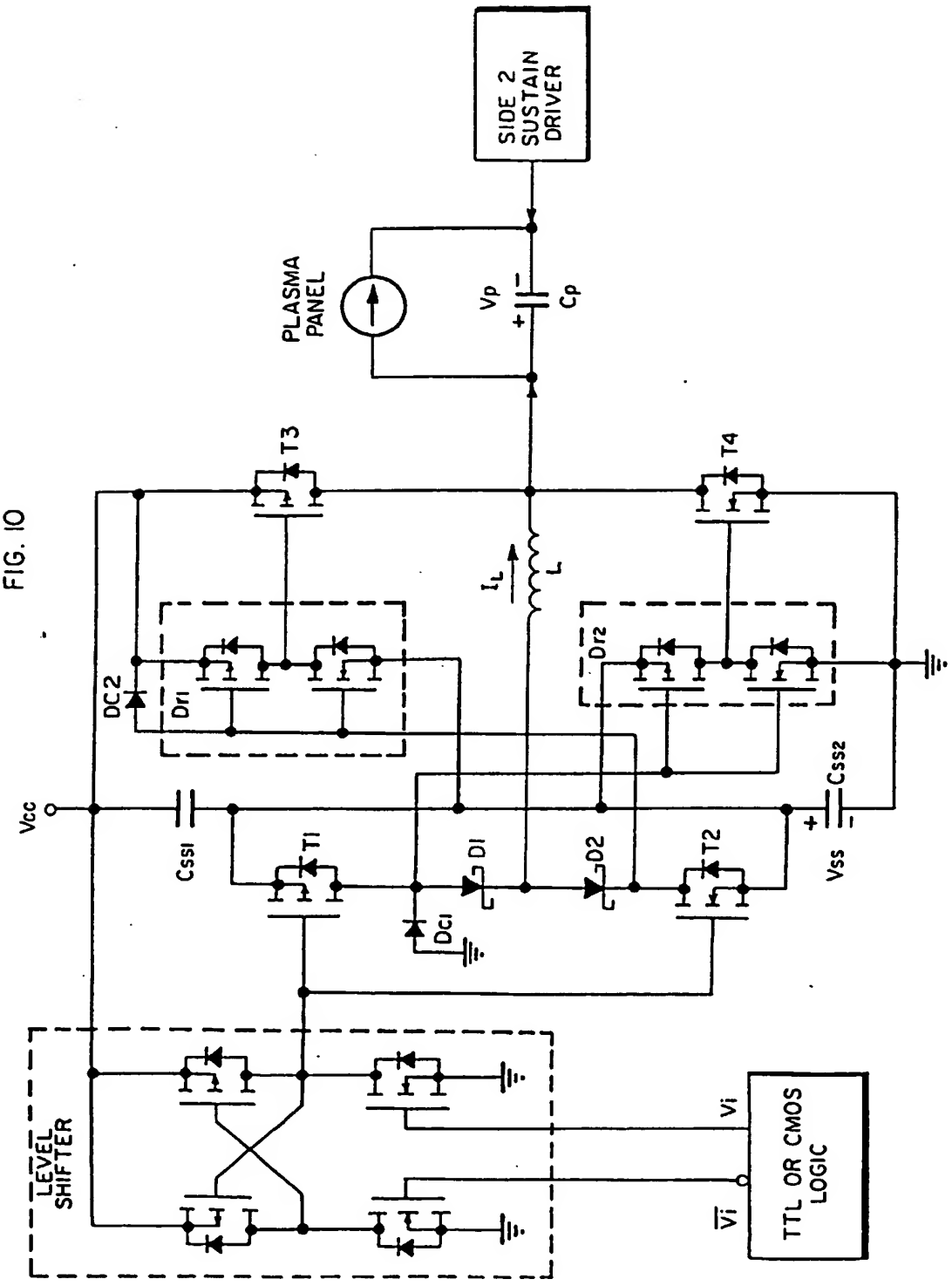

SIDE 2 SUSTAIN DRIVER
PLASMA PANEL
Vp
Cp
T3
T4
IL
L
DC2
Dr1
Dr2
Vcc
Css1
Css2
T1
T2
D1
D2
Dc1
Vss
LEVEL SHIFTER
Vi
$\overline{Vi}$
TTL OR CMOS LOGIC

FIG.11

X_{AP}

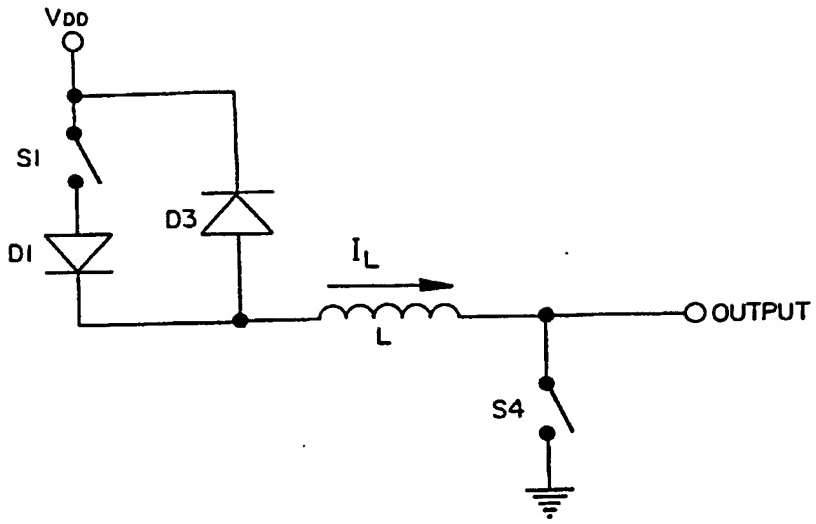


FIG. 12

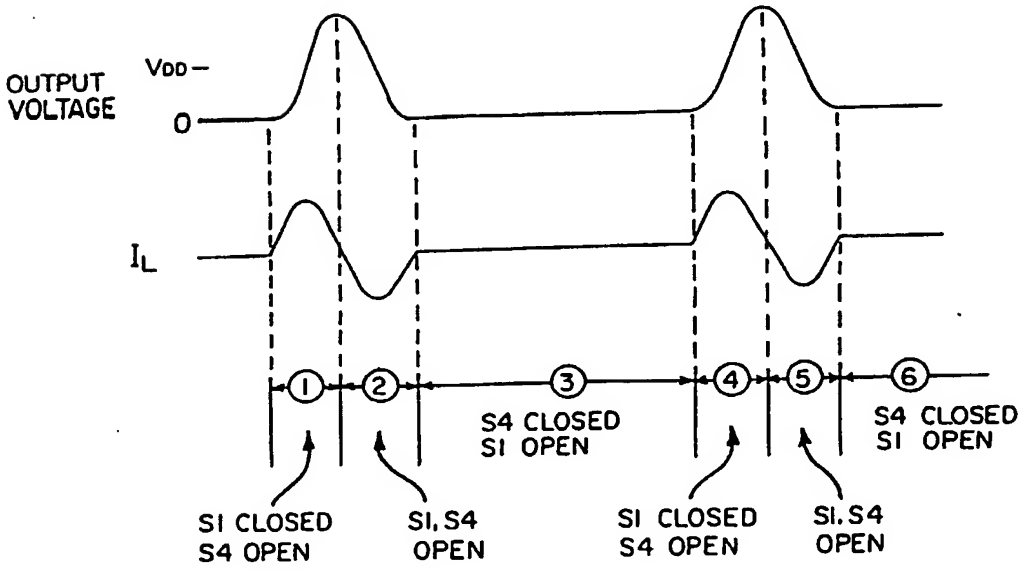


FIG. 13

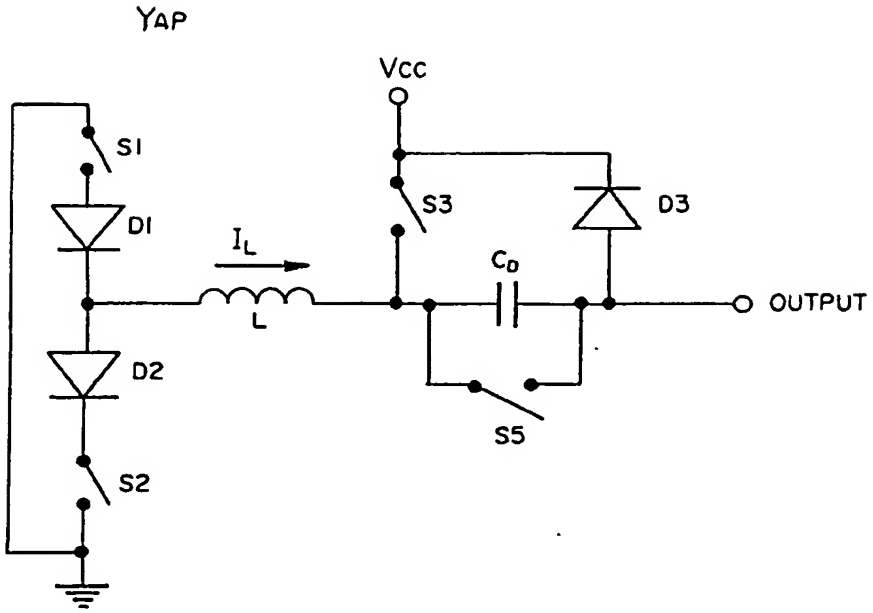
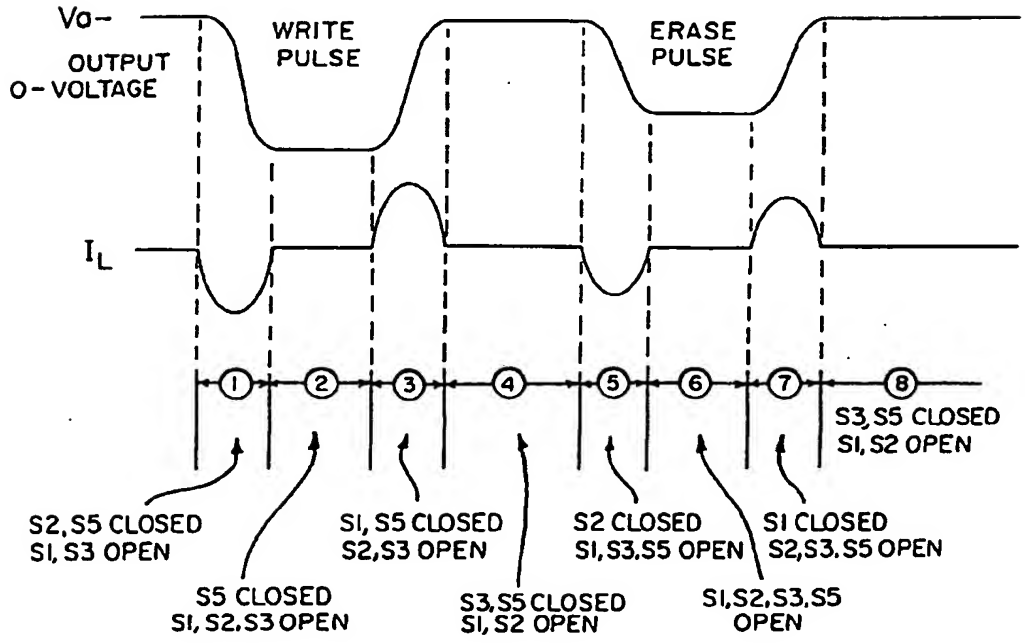

YAP
Vcc
S1
D1
S3
D3
I_L
C_D
L
OUTPUT
D2
S5
S2

FIG. 14


Vo-
OUTPUT
O-VOLTAGE
WRITE
PULSE
ERASE
PULSE
I_L
1
2
3
4
5
6
7
8
S3, S5 CLOSED
S1, S2 OPEN
S2, S5 CLOSED
S1, S3 OPEN
S5 CLOSED
S1, S2, S3 OPEN
S1, S5 CLOSED
S2, S3 OPEN
S3, S5 CLOSED
S1, S2 OPEN
S2 CLOSED
S1, S3, S5 OPEN
S1, S2, S3, S5
OPEN
S1 CLOSED
S2, S3, S5 OPEN